Filed Electronically on September 17, 2007 *PATENT*
Dkt. STL10986

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In re Application of: **Sundeep Chauhan**
Assignee: **SEAGATE TECHNOLOGY LLC**
Application No.: **10/625,386** Art Unit: **2816**
Filed: **July 23, 2003** Examiner: **Hai L. Nguyen**
For: **HIGH SPEED DIGITAL PHASE/FREQUENCY COMPARATOR FOR PHASE LOCKED LOOPS**

Mail Stop AF
Commissioner for Patents
P.O. Box 1450
Alexandria, VA 22313-1450

APPLICANT'S REMARKS FOR SECOND PRE-APPEAL BRIEF REQUEST FOR REVIEW

In reply to the final rejection of February 28, 2006 Applicant filed a Pre-Brief Request for Review on June 28, 2006. The Panel's Decision of August 30, 2006 was to reopen prosecution. The subsequent office actions of November 14, 2006 and May 17, 2007 maintained the rejections on the same grounds as that on which the Pre-Brief Panel reopened prosecution.

THE OFFICE HAS FAILED TO SUBSTANTIATE ANTICIPATION OF CLAIMS 1 AND 20 BY NOT SHOWING EVIDENCE THAT STASZEWSKI '693 DISCLOSES THE *TRANSITION LOCATION SIGNAL* RECITED BY THOSE CLAIMS

Independent claims 1 and 20 recite a *transition location signal*. During examination claims are given their "broadest reasonable interpretation consistent with the specification."[1] The "broadest reasonable interpretation" is the meaning that the skilled artisan would give to the claim term in view of the associated usage provided in the

[1] *Phillips v. AWH Corp.*, 75 USPQ2d 1321 (Fed. Cir. 2005)(en Banc); MPEP 2111

specification.[2] A construction that is inconsistent with the written description would not be arrived at by the skilled artisan, and is therefore not a "reasonable interpretation."[3]

The ordinary meaning of the disputed claim language, considering the context of which the language forms a part, is that of a signal that indicates the location of a transition. Applicant has shown that the specification provides an explicit definition of the disputed claim language:[4]

> N-bit edge detect circuit 304 outputs a single bit at the transition point of a falling edge (or rising edge, depending on the design) in the snapshot provided by N-bit parallel latch 302. This signal bit may be referred to as a transition location signal.
> (specification pg. 7 lines 7-10, emphasis added)

In support of the claimed transition location, the specification discloses a signal comparator structure employing an N-bit delay line 300 receiving CLOCK1 signal and an N-bit parallel latch 302 receiving CLOCK2 signal.[5] The N-bit delay line 300 is reset each time a transition occurs in CLOCK1.[6] The CLOCK1 transition propagates through the N-bit line 300, the status of the propagation being instantaneously observable via the respective N outputs.[7] When CLOCK2 transitions, then the N-bit parallel latch 302 captures a snapshot of the N outputs.[8] That snapshot captures the progress of the CLOCK1 transition as it propagates through the N-bit delay line 300.[9] Thus, the N-bit edge detect 304 provides a signal indicating the location of the CLOCK1 transition.

The final rejection of claims 1 and 20 is based on the Office's rationale that the snapshot signal 604 of the plurality of registers 504 in Staszewski '693 anticipates the claimed *transition location signal*.[10] However, Staszewski '693 itself clearly defines the snapshot 604 to be a timing signal, not a location signal as claimed:

---

[2] *In re American Academy of Science Technical Center*, 70 USPQ2d 1827 (Fed. Cir. 2004); *In re Cortright*, 49 USPQ2d 1463, 1468 (Fed. Cir. 1999); *In re Morris*, 44 USPQ2d 1023 (Fed. Cir. 1997)
[3] *Phillips, supra*; *In re Morris, supra*; *In re Zletz*, 13 USPQ2d 1320, 1322 (Fed. Cir. 1989)
[4] See Applicant's Pre-Brief Request pg. 2, Applicant's Response of 5/30/2006 pg. 10, Applicant's Response of 11/28/2005 pg. 14, Appellant's Brief of 5/16/2005 pg. 8, Applicant's Response of 3/15/2005 ppg. 10-11.
[5] See specification FIG. 3.
[6] Specification pg. 6 lines 23-26.
[7] Specification pg. 6 lines 12-23.
[8] Specification pg. 7 lines 1-3.
[9] Specification pg. 7 lines 3-6.
[10] See Staszewski '693 FIG. 6.

> During a positive transition (enumerated 602 in FIG. 6) of the reference clock FREF 110, each of the latch/registers 504 will be queried in order to obtain a snapshot of the quantized fractional phase difference between the dVCO 104 clock signal CKV 114 phase and the reference clock FREF 110 signal phase. (Staszewski '693 col. 8 lines 30-36, emphasis added)

> During a positive transition 602 of the reference oscillator FREF 110, the plurality of latch/registers 504 are accessed to obtain a snapshot 604 of the delayed replicas of the dVCO clock CKV 114 relative to the rising edge of the reference oscillator FREF 110. The snapshot 604 can be seen to express the time difference as a digital word. (Staszewski '693, col. 8 lines 45-46)

FIG. 6 of Staszewski '693 clearly defines the snapshot signal 604 as a multi-bit word, each bit being associated with the state of a respective delayed replica D(n) of the oscillator 104 (dVCO) pulse CKV 114. The skilled artisan readily recognizes that the snapshot signal 604 indicates a timing difference between the FREF transition 602 and the CKV 114. The snapshot signal 604 cannot define the location of the transition 602 because Staszewski '693 does not synchronize any reference point associated with a transition of CKV 114.

Applicant has shown that the snapshot signal 604 is irrespective of transition 602 location because there is a plurality of different locations that the transition 602 could occur and yet produce the same snapshot signal 604. For example, the following marked-up FIG. 6 of Staszewski '693 illustrates that the snapshot signal 604, in and of itself, cannot differentiate between whether the transition 602 is leading or lagging the CKV 114. That is, the same snapshot signal 604 exists both at multiple locations prior to the CKV rising edge and at multiple locations following the CKV falling edge:

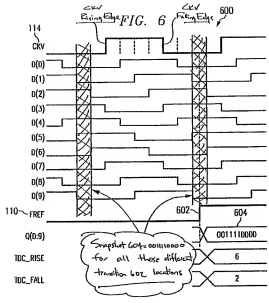

FIG. 6

The skilled artisan readily understands that Staszewski '693 discloses employing the snapshot signal 604 to determine a phase difference between FREF and CKV, and then compensates for the phase difference in a manner described by equations 8-13.[11] The skilled artisan also readily understands that the present embodiments as claimed determines a *transition location signal*, as discussed above, and then from the transition location signal derives a numerical phase difference value via the N-to-M weighted encoder 306 in FIG. 3 discussed above.[12]

Therefore, the skilled artisan would conclude that the Office's interpretation of *transition location signal* to include the phase difference of the signals being compared is inconsistent with both the ordinary meaning of the phrase and the usage of the phrase in the specification. As such, the Office's construction of *transition location signal* is not within the broadest reasonable interpretation consistent with the specification, and as such cannot sustain the present anticipatory rejection. Applicant respectfully believes that the rejection of claims 1 and 20 and the claims depending therefrom should be reversed because the Office has not substantiated evidence that Staszewski '693 discloses the *transition location signal*.

[11] Staszewski '693 col. 8 lines 50-55.
[12] Specification pg. 7 lines 11-13.

THE OFFICE HAS FAILED TO SUBSTANTIATE ANTICIPATION OF CLAIM 10 BY NOT SHOWING EVIDENCE THAT STASZEWSKI '693 DISCLOSES THE *ENCODING CIRCUITRY* RECITED BY THAT CLAIM

Independent claim 10 recites *encoding circuitry*. The Office's rationale for the rejection is that the NORM circuit of Staszewski '693 anticipates the *encoding circuitry* of claim 10 because it "converts the input digital signal into its equivalent binary code."[13]

The rejection is without merit because Applicant has shown that the passage on which the Office relies neither discusses the NORM circuit nor discloses anything that "converts the input digital signal into its equivalent binary code."[14] The rationale for the rejection appears to be based upon a misplaced characterization of the cited reference. Applicant has also shown that the NORM (normalization) circuit of Staszewski '693 alters the input value quantitatively, not qualitatively, and that as such the skilled artisan would readily understand that the NORM circuit of Staszewski '693 is not even within the ordinary meaning of what is referred to as an "encoding circuit."[15]

Therefore, the skilled artisan would conclude that the Office's interpretation of *encoding circuit* to include the normalization circuit of Staszewski '693 is inconsistent with both the ordinary meaning of the phrase and the usage of the phrase in the specification. As such, the Office's construction of *encoding circuit* is not within the broadest reasonable interpretation consistent with the specification, and as such cannot sustain the present anticipatory rejection. Applicant respectfully believes that the rejection of claim 10 and the claims depending therefrom should be reversed because the Office has not substantiated evidence that Staszewski '693 discloses the *encoding circuitry*.

Respectfully submitted,

By: _____

Mitchell K. McCarthy, Registration No. 38,794
McCarthy & Associates
500 West Main, Suite 609
Oklahoma City, Oklahoma 73102

---

[13] Office Action of 2/28/2006 pg. 8, citing Staszewski '693 col. 5 line 64 to col. 6 line 43; repeated in Office Action of 5/17/2007 pg. 7.
[14] Applicant's Response of 2/14/2007 ppg. 11-13; Applicant's Response of 5/30/2006 ppg. 14-17; Applicant's Response of 11/28/2005 ppg. 18-20.
[15] *Id.*